# Process window analysis of post OPC SRAF placement

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## *Abstract*

RET such as OPC, Sub-resolution assist features (SRAF), is used for improve process window, especially for semi-dense and isolated patterns. Traditional studies about SRAF is always around target main pattern and SRAF, but OPC can change the shape of target pattern, so this paper is investigated the relationship between process window and post OPC SRAF placement. The OPC model is optical model and resist model of synopsys, and use slitho as simulation tool to get process window data.

**Keywords—Sub-resolution assist features (SRAF), OPC, process window, SRAF placement.**

## *Introduction*

When attempting to progressively shrink the critical dimension (CD) of a device by applying Moore's Law, resolution enhancement technology (RET) must be implemented to improve the quality of images projected on the photoresist. However, OPC alone cannot guarantee an effective increase in the process window, and can even lead to reduced processing efficiency. Therefore, sub-resolution assist features (SRAFs) must be insert to further increase the process window.

As we all know, SRAF is insert around main pattern before OPC. Traditional SRAF is insert by rules, The best SRAF space value has been recommended through experiment and optical intensity, using isolated line or contact, but this value is only suit for isolated patterns, there are lots of random and semi-dense pattern in full chip. Many studies are done for SRAF of random patterns like Genetic Algorithm and Model-Based Scattering Bars Implementation, but both of them focus on SRAF around target before OPC. However, OPC can change the shape of main pattern, in other words, the width of SRAF, the space between SRAF and main pattern can be changed after OPC, so they may not suitable for post OPC pattern. It`s easy to understand, we can control the width and space of SRAF easily, but hard to control the space between SRAF and post OPC pattern;

In this paper, we build optical model and resist model (OPC model) using synosys`s tool, for 65nm contact layer, this model is used for OPC correction. At the same time, we build optical model on slitho tool (slitho model ) using the same condition with OPC model, this model is used for process window simulation. First, we will add different space SB for isolated contact, run OPC using OPC model, then calculate process window of all isolated contacts using slitho model, and find the best space for biggest process window. Second, we use the same way on regular semi-dense pattern (single Row), these semi-dense pattern has same width but different space, we aim to find the relation between SRAF space and main pattern pitch. Finally, we select some patternand put on wafer, calculate the final wafer process window to verify this relation.

## *CONCLUSION*

This study developed the relationship between post OPC SRAF space and process window. From these experiments, we can get some useful information. Best post OPC SRAF space for isolate contact may not be best for semi-dense or random contacts. For semi-dense and random contact, there is a post OPC SRAF range which can keep process window within ±10%, and below a certain value process window has high risk, we can obtain these space range or certain value by experiment. In actual production, we can`t control post OPC SRAF at a fixed placement, but we can keep these SRAF at a certain range to improve process window.

## *Experiment AND Results*

First, we adopt traditional way to find best SRAF space. As fig. 1 shows, Space X1 is space between SRAF and isolated contact, this space is a variable value from 40nm to 600nm. Space 2 is space between first SRAF and second SRAF: 90nm, width 1 is width of first SRAF: 40nm, width 2 is width of second SRAF: 35nm, main pattern target is 106nm. After OPC correction, process window show as fig. 2 by using slitho model. This process window is represent by common DOF combined with anchor pattern (Dense target 106nm, space 64nm) at 4% EL, just like fig. 4 shows. As we can see from this trend, There is a max DOF at SRAF space 114nm, so the best SRAF space for isolated contact is 114nm. Of course, this space is post OPC space, instead of before OPC (this space is 120nm before OPC).

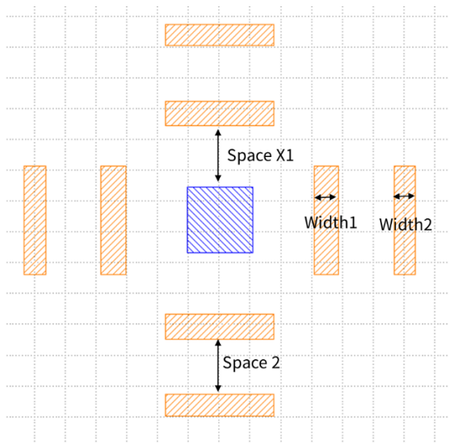


Fig. 1. Isolated contact

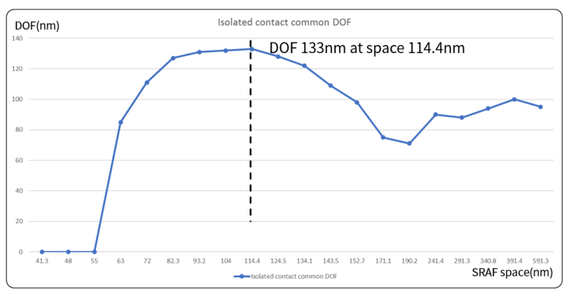


Fig. 2. PW trend with SRAF space

Fig. 3 shows the intensity of SRAF space 55nm and 114nm, SRAF space 114nm has better slope than SRAF space 55nm. On the other hand, though SRAF space 55nm is closer to main pattern, it`s intensity no higher than SRAF space 114nm.

For isolated contact, space of post OPC SRAF is close to space of before OPC due to it`s symmetry. However, when it`s asymmetric, the gap will be much bigger just like fig. 4 shows. The post OPC SRAF space becomes to 60nm from 100nm before OPC. In order to find the best post OPC SRAF space, we do the same experiments for these semi-dense patterns, whose SRAF space are from 40nm to 300nm. Semi-dense pattern space are 120nm, 140nm, 170nm, 190nm respectively. Fig. 6 shows the results of trend between post OPC SRAF space and common DOF with anchor. It`s clear that there is no one SRAF space that always keep biggest DOF like isolated contact. Instead, there is a post OPC SRAF range from 69 ~ 141nm which the DOF is relatively stable about within ±10%, as black dotted line area shows in fig. 6. Another result we can see from fig. 6 is, when post OPC SRAF space is less than 55nm, there is no common process window.

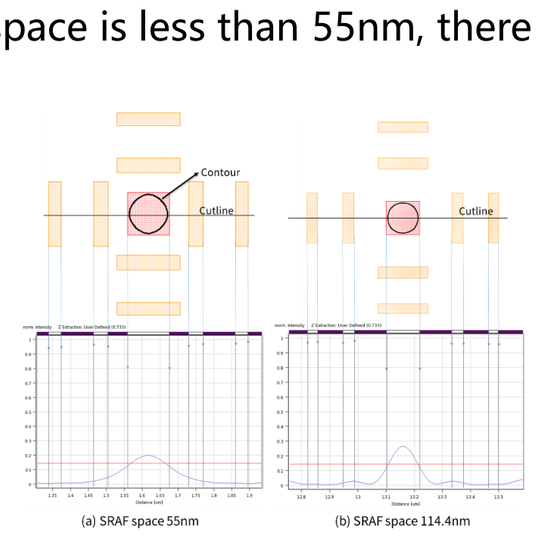


Fig. 3. Intensity of isolated contact

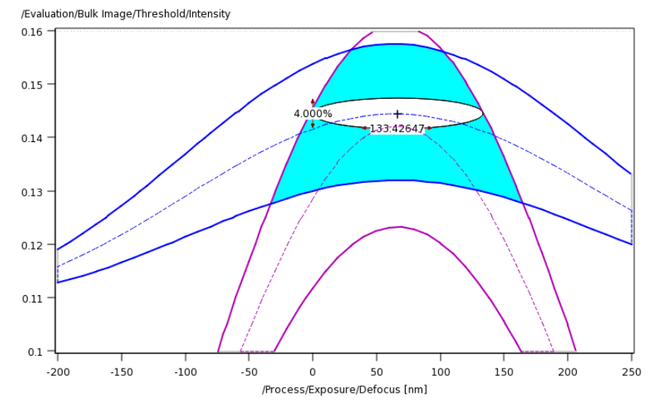


Fig. 4. PW of SRAF space 114.4nm

In the final experiment, we select three random pattern in real full chip show in fig. 7. Post OPC SRAF space range are from 26.9nm to 189.5nm, Results are show in fig. 8. Similar to semi-dense pattern, there is a post OPC SRAF range from 60 ~ 105nm which the DOF is relatively stable about within ±10%, as black dotted line area shows in fig. 8, which wafer data also proved this point. In addition, post OPC SRAF less than 55nm has no window.

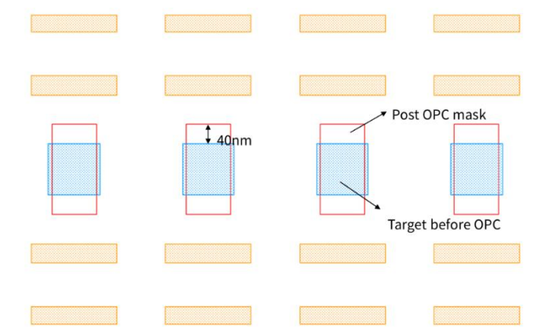


Fig. 5. Semi-dense pattern

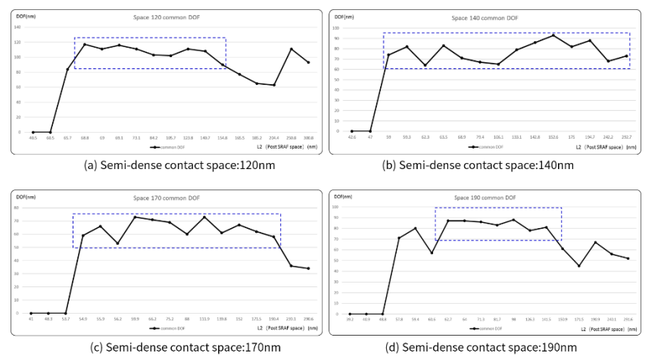


Fig. 6. PW trend with SRAF space

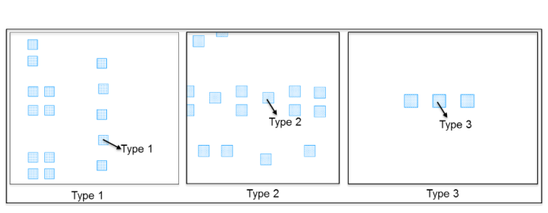


Fig. 7. Three type pattern.

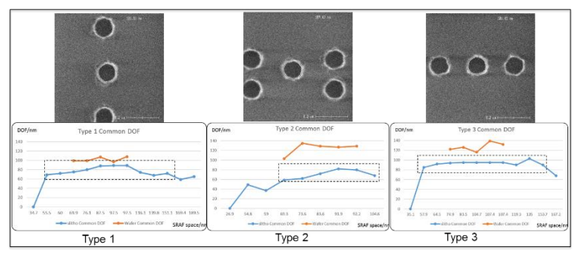


Fig. 8. Three type pattern wafer image and PW trend