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Uniformity of device performance improvement for the SOT-MRAM by optimizing the lithography process at 200-mm-wafer manufacturing platform

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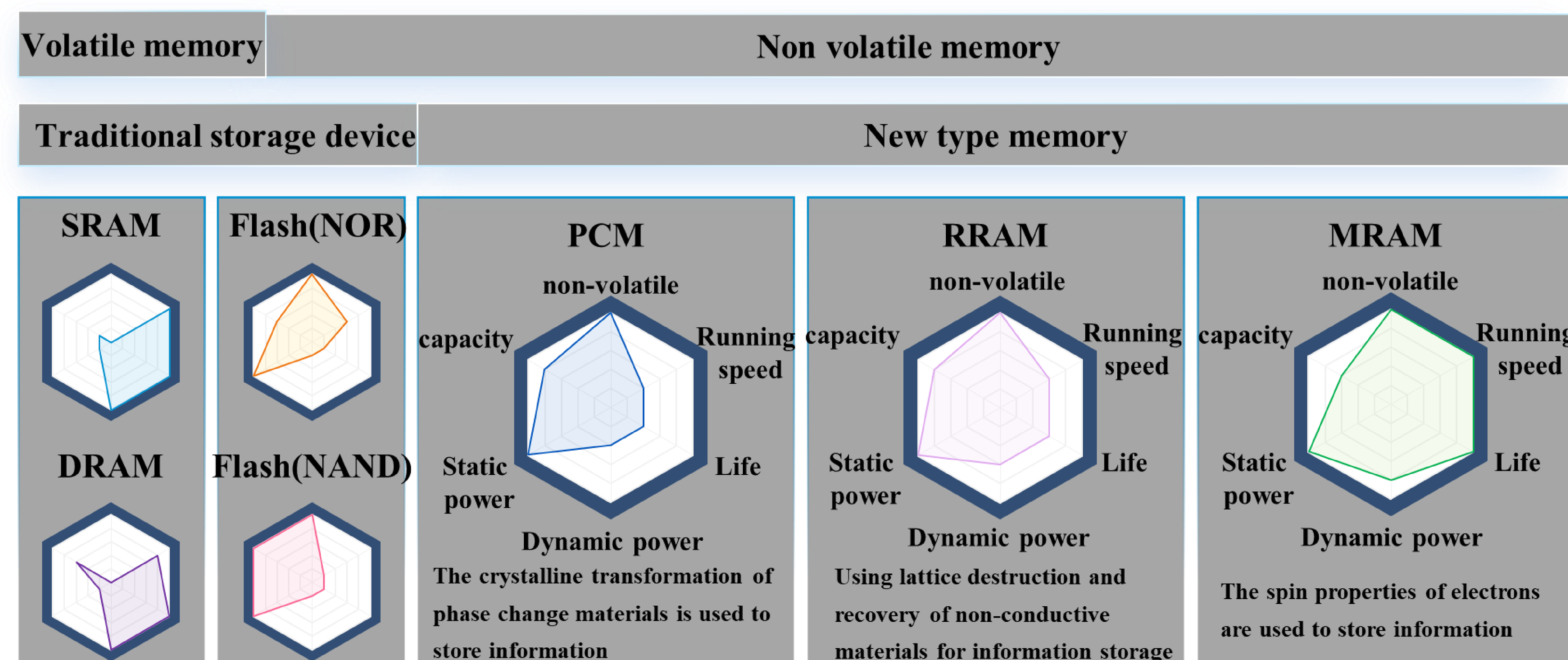
Abstract

We examined the influence of process uniformity on the device performance for the spin-orbit torque (SOT) magnetic random access memory (MRAM) devices. By optimizing the lithography process, in particular, through changing the multi-energies exposure compensation and pretreatment in developing, we demonstrated 1.6 times sigma improvement of the critical dimensions (CD), leading to 49.5%, 54.2%, and 63.2% sigma% reduction for SOT channel resistance (Rb), magnetic tunnel junction (MTJ) resistance (Rmin) and switching current (IC) respectively. These promising results will help to deliver SOT-MRAM to the mass manufacturing in the semiconductor industry.

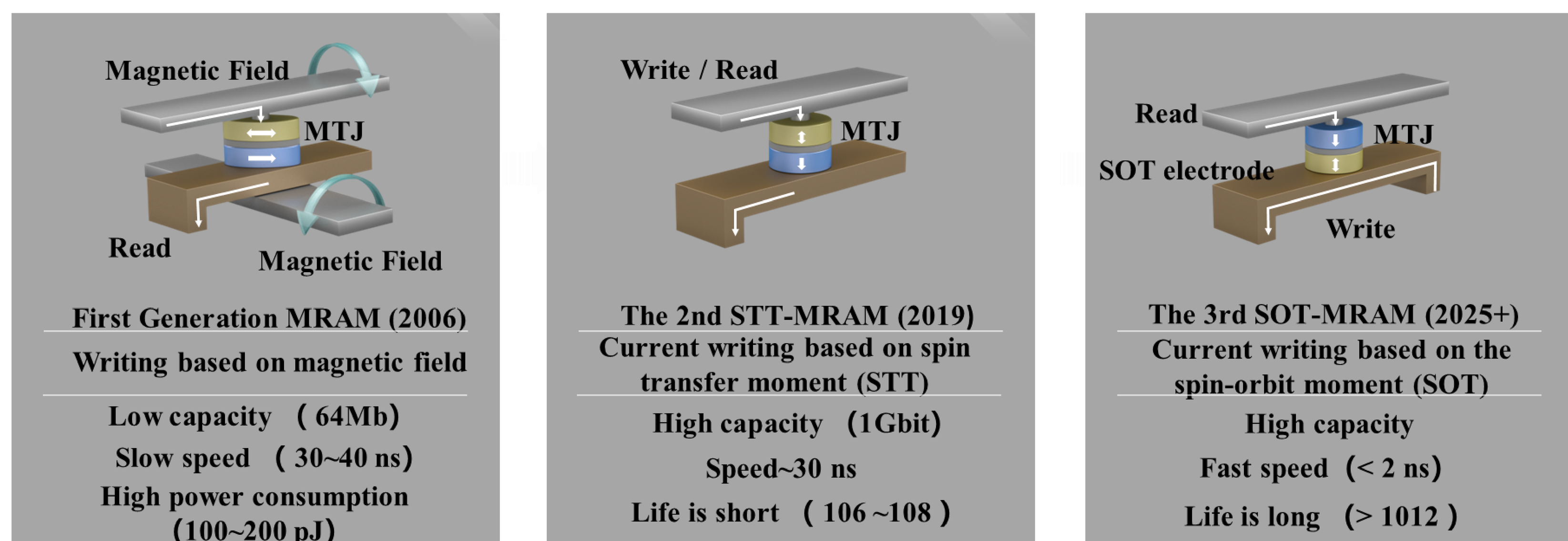
Characteristic of new storage

Magnetic random access memory (MRAM), as an emerging non-volatile memory, features high read and write speed, high endurance, long storage time and low-power dissipation, which has captured great interest in the semiconductor industry [1].

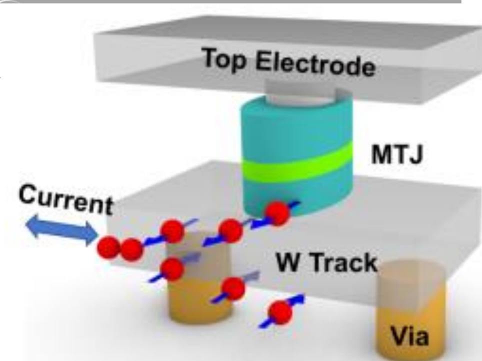


Advantage of SOT MRAM and 1 bit MTJ cell

Spin-transfer torque (STT) MRAM, an important segment of MRAM, has been in the mass production phase since 2019, which is used as a replacement for embedded Flash memory [2]. However, it is hard to replace the L1 or L2 SRAM cache due to the speed and the endurance dilemma [3].



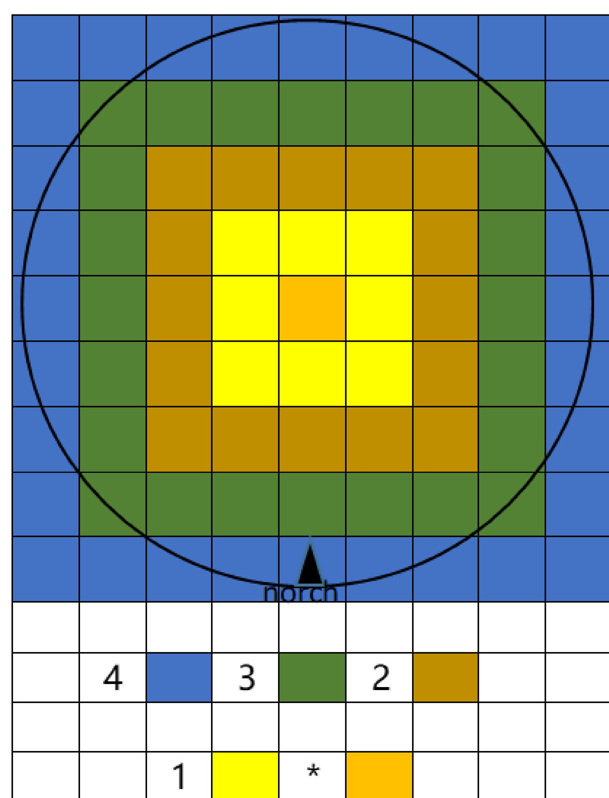
The 3rd generation MRAM, Spin-orbit torque (SOT) MRAM, a three terminal device structure, in which the read and write paths are separated. In such a case, the write current does not go through the tunnel barrier, which would not degrade the quality of the tunnel barrier as happened in the STT-MRAM.



Current problems and lithography solutions

It is still not clear how the process uniformity would influence the SOT-MRAM device's performance. Therefore the purpose of our study is to investigate the effect of process uniformity on the devices characteristics.

In order to do so, multi-energies exposure compensation was used to expose different areas of the wafer with different energies to compensate for the poor uniformity of CD caused by the uneven substrates, as shown on the right. Different colors represent different energy values on the wafer. On the other hand, a pretreatment was introduced with chemical through changing the developing process. With the above-mentioned methods, the sigma can be improved by 68.4% and 54.2% for the MTJ CD and the SOT channel CD respectively.



Schematic diagram of multi-energies exposure

Results and Discussion

The electrical data of the fabricated devices, such as Rb (SOT channel resistance), Rmin (MTJ resistance), and IC(critical switching current), are shown in Figure 1 (a) to (c). As can be seen, after improving the uniformity of the device's CD, Rb, Rmin, and IC are all significantly reduced, and the distributions of each parameter are decreased as well (the detailed data are listed in Table 1). At the same time, the decreasing trend of the critical switching current is more obvious due to the reduced shunting current effect [4,5]. Most importantly, the distributions become much tighter than those of POR (sigma% reduced to 49.5%, 54.2%, and 63.2%, respectively, for the Rb, Rmin, and IC). The reduction of the switching current and the distributions would assist SOT-MRAM in attracting interest from semiconductor foundries, making it mass production in the near future.

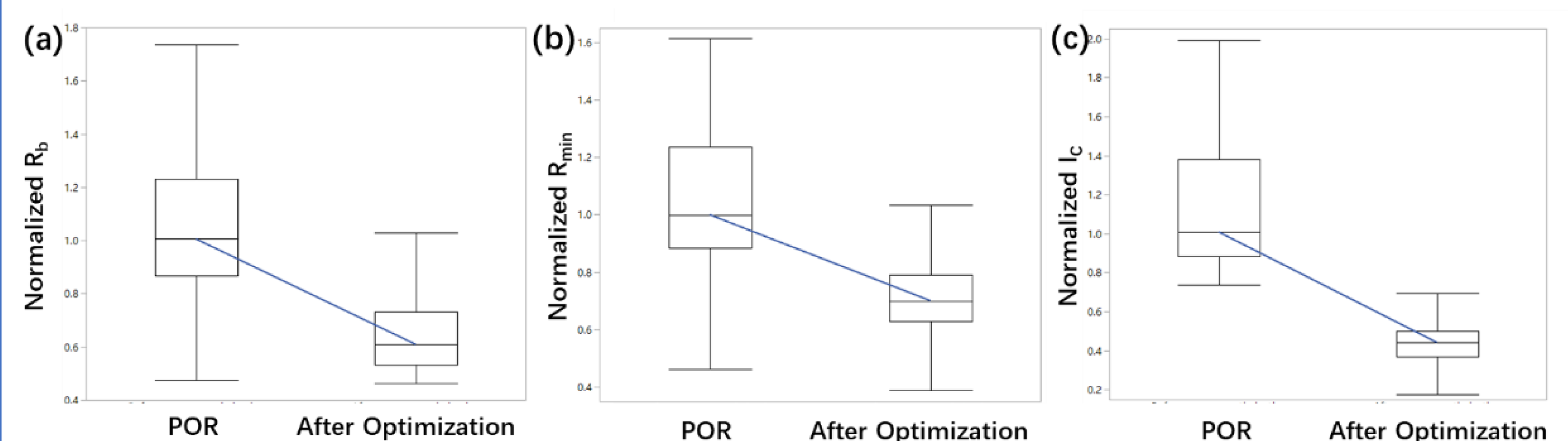


Fig.1 (a) SOT channel resistance, 1(b) junction resistance and 1(c) switching current comparison between POR and that after process optimization. The data are normalized by median values of each parameter of the POR process.

Parameters	POR		After Process optimization	
	Median	Sigma	Median	Sigma
Rb (SOT channel resistance)	1	0.29	0.66	0.15
Rmin (MTJ resistance)	1	0.23	0.70	0.10
IC (switching current)	1	0.27	0.43	0.10

Table.1 Comparison of SOT channel resistance, MTJ resistance and switching current for POR and the optimized process (the data are normalized by the values of each parameter of the POR process).

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