Designing high quality test chips with improved coverage for design rule exploration, process variation improvement and hotspot discovery

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ABSTRACT

A key challenge to new IC technology node development is the lack of quality and comprehensive layout that can effectively probe process capabilities, design and process interaction and disclose stress DR corners. At the very first stage of process development, process specifications need to be defined, RET (Resolution Enhancement Technique) recipes need to be specified, and design rule establishment is required to validate layout manufacturability. Each of these key works requires the availability of chip layouts to evaluate the quality, accuracy, and comprehensiveness of development results. This is a classic "chicken-and-egg" dilemma, we need layouts in order to develop the process, however, we also need as much information of the process and design rules, if not only a snapshot, before meaningful chip layout design could be carried out.

An abundant variety of layouts shall be established, which would cover a span of design styles, in order to develop and test RET recipes and design rules properly. Yet, IC designers do not start developing layouts until AFTER actual process development has progressed, to a certain point that reasonable amount of understandings on manufacture capabilities and limitations are comprehended, and the ground design rules are appropriately established. Even then, it is only possible to get limited number of design layouts until further process maturity.

In this work, we propose a synthetic layout generation methodology which delivers design patterns based on only ground design rules. The wide range of design patterns could be tested and evaluated to gain abundant information of the process, disclosing strengths and limitations, even before the manufacturing phase. This new approach brings high quality process development with remarkably reduced process development cycle time.

INTRODUCTION

Traditional methods of migrating previous node QA patterns, manually crafting new testcases, and targeted-pattern generation leave gaps in process qualification coverage on new technology nodes. To solve this critical problem, we deploy synthetic layout generation to produce layouts that cover vast design space, delivering all variety of design patterns from simple to complex topologies and wide ranges of geometric variations.

With this synthetic layout generation, it is possible to generate layouts with an array of characteristics including detection on 1D or 2D routing, evaluation on the amount of non-preferred-direction routing desired, wires of a variety of lengths and widths, patterns with targeted density ranges which vary on tip-to-tip and tip-to-side spacings, VIAS with different enclosures, and all other ranges of characteristics needed to probe process capabilities. Quality patterns with high coverage are evaluated by process simulation and/or testing on manufactured test chips with the process of interest. It is also possible to generate vast pattern sets and pattern styles which enable practical early testing. Litho simulation and/or test chip silicon metrics are able to reveal hotspot with bridging and pinching patterns, contour edge roughness, process variation severeness, as well as design rule boundaries. By swift and early discovery on process strengths and limitations, it gives clear direction for RET optimization and DR(design rule) refinement opportunities for further process optimization. This approach brings high quality process development with remarkably reduced process development cycle time.

SYNTHETIC LAYOUT GENERATION APPLICATION

LSG Synthetic Layout Generator generates guided random layouts that are design-like and adhere to specified design rules. The randomness is achieved by applying Monte Carlo methods during pattern construction.

Figure 1. LSG Synthetic Layout Generation

Design rules and style guidelines are applied as constraints during selection and placement of unit patterns into a layout grid. The rules determine what unit patterns can be placed at a layout grid given the knowledge of surrounding unit patterns. Weighting constraints can be applied to give priority preferences for specific unit patterns.

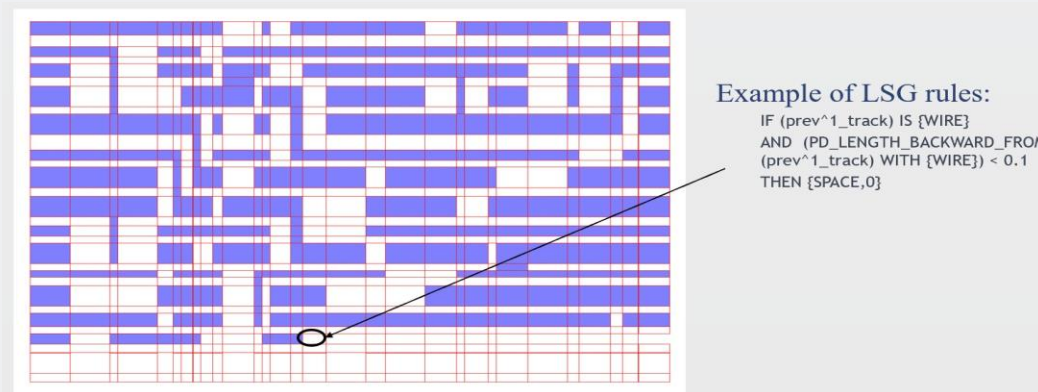


Figure 2.Applying LSG Rule to Layout Generation

LSG generates a variety of design styles that covers wide design space. The synthetic layout generator produces numerous patterns, which are under the defined rules and dimensional constraints. Configurations are made to generate either 1D or 2D designs, and to control percentage ranges of preferred direction and non-preferred direction wires, specify ranges of wire widths, lengths, and density ranges. LSG takes all these constraints into account to generate simple patterns as well as complex corner cases that are difficult for human test design to cover comprehensively.

We utilize quick and effortless LSG parameter tuning to stress DR conditions, generating random patterns that present complex and varied relations of multiple min features combined together. An example is illustrated in Fig. 3.

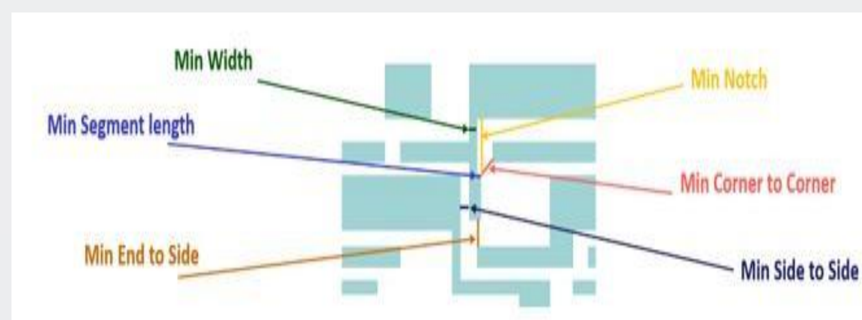


Figure 3. LSG pattern combining multiple min features

NEW TECHNOLOGY NODE PROCESS SPECIFICATION

At the very first stages of process development, process specifications need to be defined, RET recipes need to be specified, and design rule establishment is required to validate layout manufacturability. Technology node architects may envision several candidate process specifications. At this beginning stage, there are no RET recipes and no DRC (design rule check) decks. Architects desire to evaluate the feasibility and effectiveness of multiple combinations of layout conditions. They envision a handful of key design rules and want to explore sets of constraint values for these rules. Each set is a process specification candidate. We apply LSG to produce synthetic test layout for each process candidate. We create rough RET recipes to test our high-level hypothesis and converge on one optimal process candidate

DEVELOPING RECIPES FOR THE PROCESS SPECIFICATION

Upon choosing the optimal process candidate, we dive deeper into RET recipe evaluation, exploring limitations of the chosen architecture, and discovering ways to improve manufacturing process. At this stage, we generate more complex patterns and greater coverage and dimensional variations to trigger and observe more pattern-process interaction. We perform virtual testing based on RET simulation results and we place patterns onto test-chips to measure manufactured silicon results. Simulated and measured results would guide us in refining the process spec, determining ground rules, and/or making process specification and DR constraint tradeoffs. This is an iterative process to "add/remove/refine DR => generate synthetic layout => test and refine RET => measure and evaluate results => add/remove/refine DR".

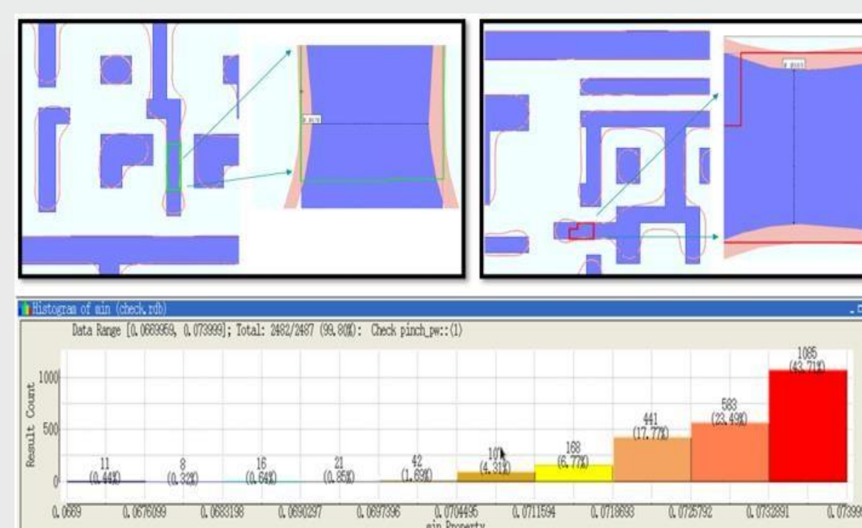


Figure 4. Sample Pinching Hotspots

In Fig. 4, we show samples of pinching hotspots in LSG-generated test layout. The layout snippets show the DRAWN layout (shown in blue) as intended by the layout designer. The RET simulated contours (shown in pink) give an accurate prediction of how the layout will print onto silicon. The two examples show metal pinching to less than the desired manufactured width. The histogram shows the distribution of pinching severity for patterns with predicted manufacturing defects. Process engineers evaluate these results to determine corrective action for improving the process, avoiding such defects in following manufacture phase.

Process effects can impact individual layers or a combination of layers. An example of a VIA-overlap hotspot is shown in Fig. 5. The RET-simulated contours (shown in purple) show the predicted line-end pull-back. The pull-back reduces the connection area between the metal and VIA by 30% - 50%, leading to severely compromised electrical connectivity and robustness of this pattern. With this early finding, process engineers evaluate the testcase to identify corrective action for the next process improvement iteration.

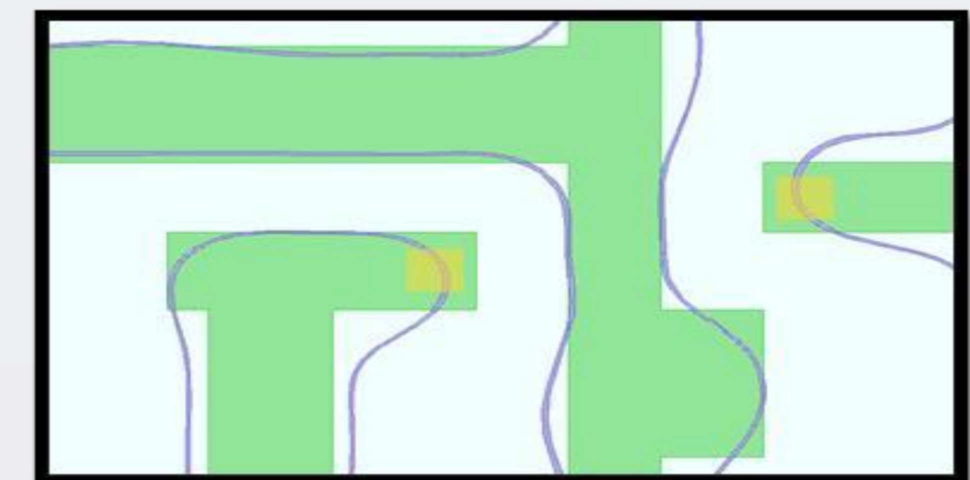


Figure 5.VIA Enclosure Hotspot -- Poor Metal-to-Via connection

ESTABLISHING DESIGN RULES

Synthetic test case generation provides layouts to test and refine the process spec, optimize RET recipes and to establish design rules. Design rules are codified into a Design Rule Manual. DRC (design rule check) rule sets are written to validate that layouts are under required constraints. Separate teams will focus on building production-ready DRMs and DRC decks. Corresponding QA team qualify their results before release. LSG layouts assist QA teams to thoroughly test DR run sets for release qualification.

Synthetic layout generation can produce thousands of test cases to qualify individual design rules in a flow that generates expected-to-fail and expected-to-pass test patterns. The expected-to-fail patterns are generated with an error marker indicating expected-failure-locations. After running DRC on the LSG generated test layouts, differences between DRC run results and expected-to-fail patterns reveal DRC MISSED violations; differences between DRC run and expected-to-pass patterns reveal DRC FALSE-POSITIVE violations.

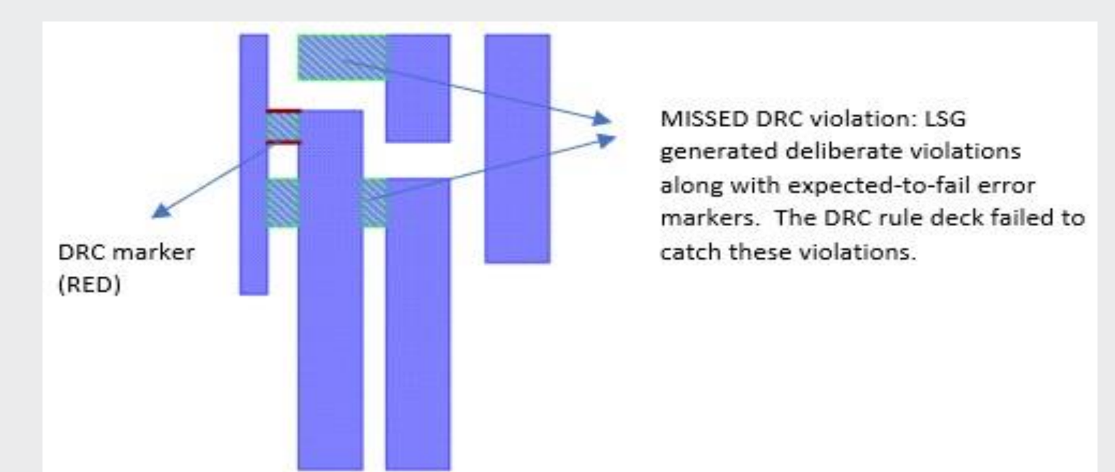
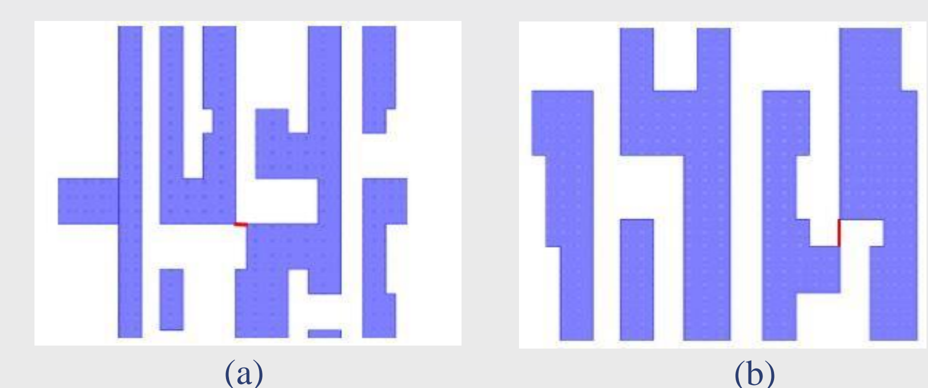


Figure 6. LSG Synthetic Layout Generation

The synthetic layout generator also generates large layouts to test all the DR's combined together with their interdependencies and to validate their correctness in complex conditions. As shown in Figure 6 and 7.



(a) (b)

Figure 7. False error (a) End-to-Side spacing (b) End-to-End spacing

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