A Via/Contact Layout Decomposition Method for Directed Self-Assembly Based on Local Optimization

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INTRODUCTION

Directed self-assembly (DSA), based on block copolymers (BCP), as a new "bottom-up" lithography technology, has a different principle from traditional optical lithography. Because of the inherent advantages of low cost, high resolution, and high yield without a light source, DSA is rapidly gaining widespread attention. The semiconductor industry regards DSA as a next-generation lithography technology. Although DSA has made great progress in technology, the design method of DSA via/contact decomposition is not satisfactory. Therefore, a high-quality via/contact layout decomposition method is required to enable the technology.

Template limit

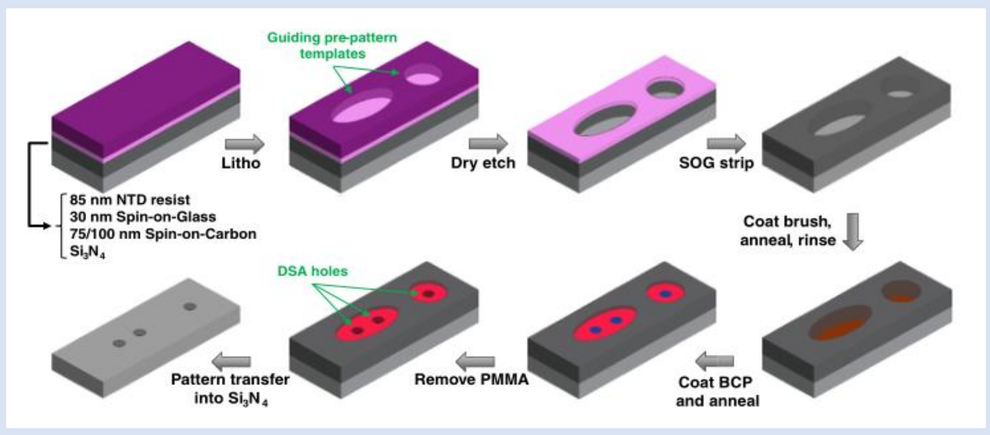


Figure.1. Schematic overview of templated DSA process flow[1].

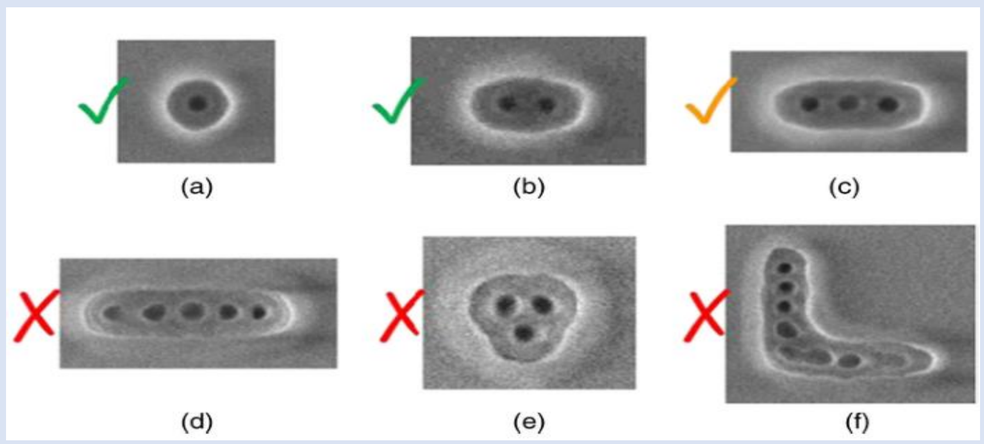
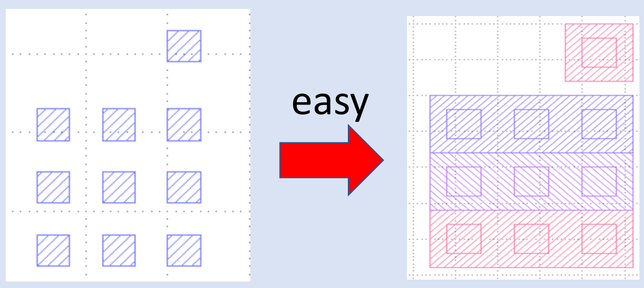


Figure.2. SEM images of DSA hole formation for various template shapes[2].

The figure.1 shows the process flow of DSA technology. It can be concluded that if you want to use DSA technology to process the chip via layer, you must determine the corresponding guide template.
The figure.2 shows various configurations of DSA holes obtained in different templates. It is indicated that it limits the pattern types considered in the actual implementation of DSA to "singlets", "doublets" and "triplets".

Calculation complexity limit



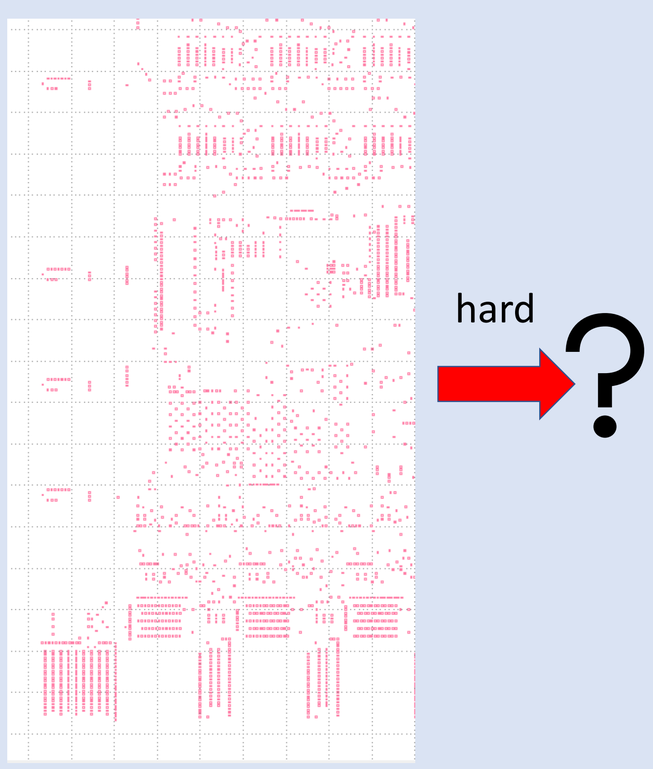


Figure.3. A simple comparison of optimal solutions for different scale layouts.

The figure 3 is a simple comparison of algorithms for different scale layouts. Most algorithms can easily get the optimal solution for small-scale layout, but cannot deal with large-scale layout. Therefore, there is a need in the art for technology via grouping and splitting with low computational complexity and high grouping quality.

DESIGN METHOD

A. Layout Split

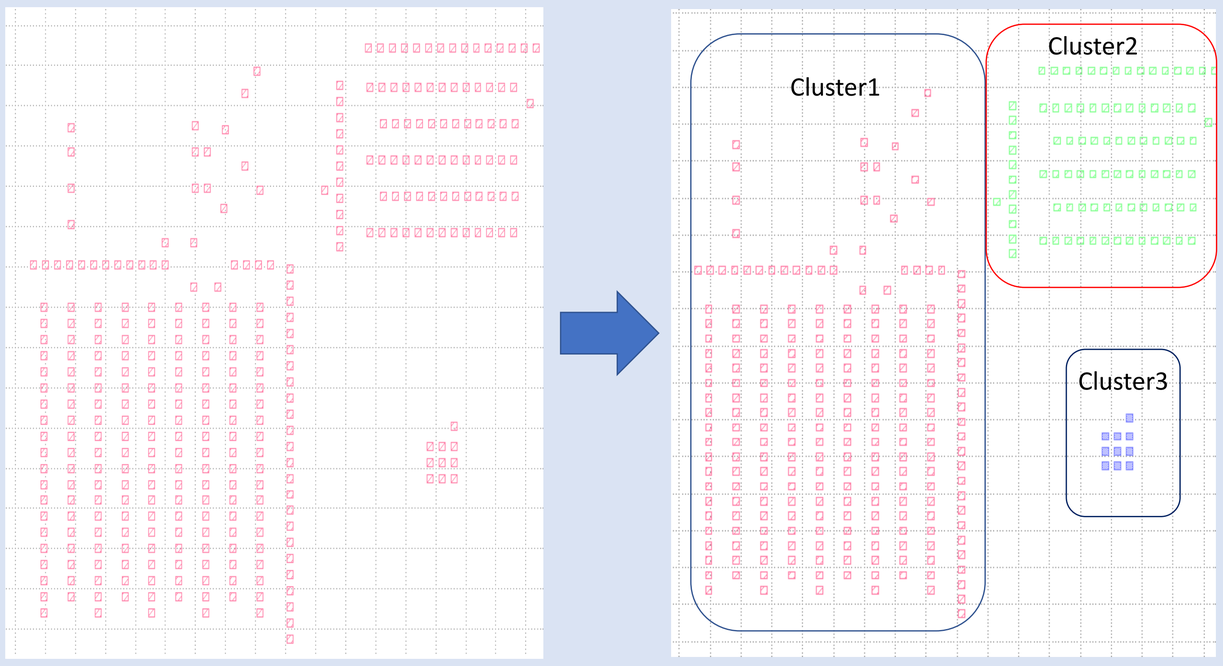


Figure.4. Schematic illustration of noncolor-conflicting via clusters.

It is almost impossible to find a good solution in a limited time in a large practical circuit with tens of thousands or hundreds of thousands of vias. Therefore, a simplified algorithm is needed to reduce the computational complexity. The figure.4 shows the workflow of the layout split, which can effectively reduce the computational complexity.

B. Local optimization algorithms

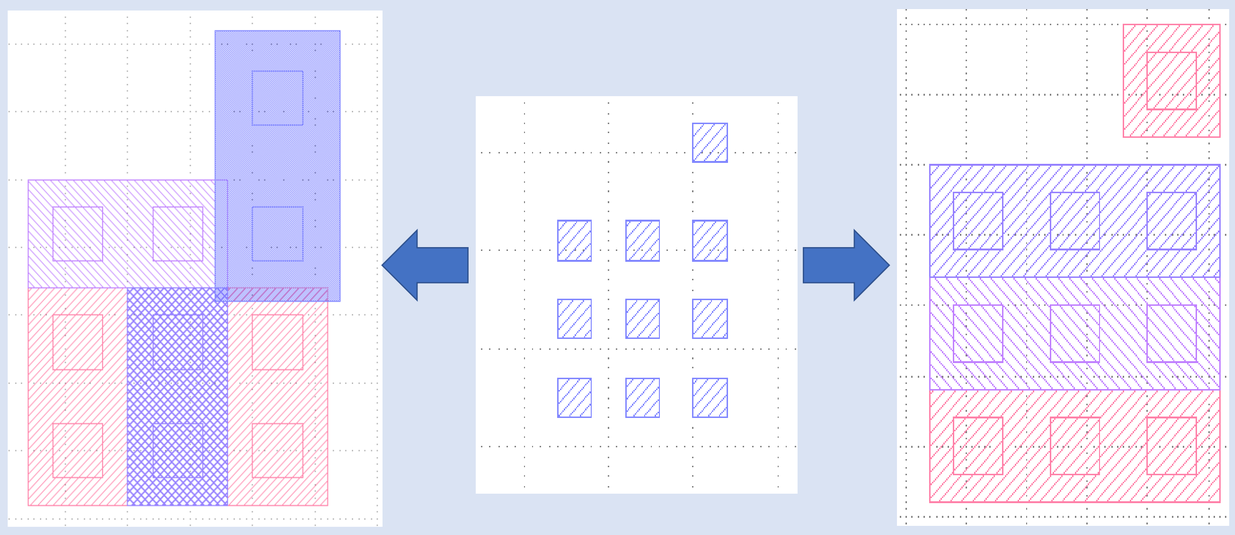


Figure.5. Grouping and coloring results of the same cluster under different grouping schemes. On the left is the maximum cardinality matching only, and on the right is the local optimization.

The figure.5 shows the grouping and coloring results of the same cluster under different grouping schemes. It shows that simply using maximum cardinality matching cannot deal with the conflict between groups. After adding local optimization, the conflict between groups can be significantly improved, to reduce the number of colors and make the results better.

RESULT

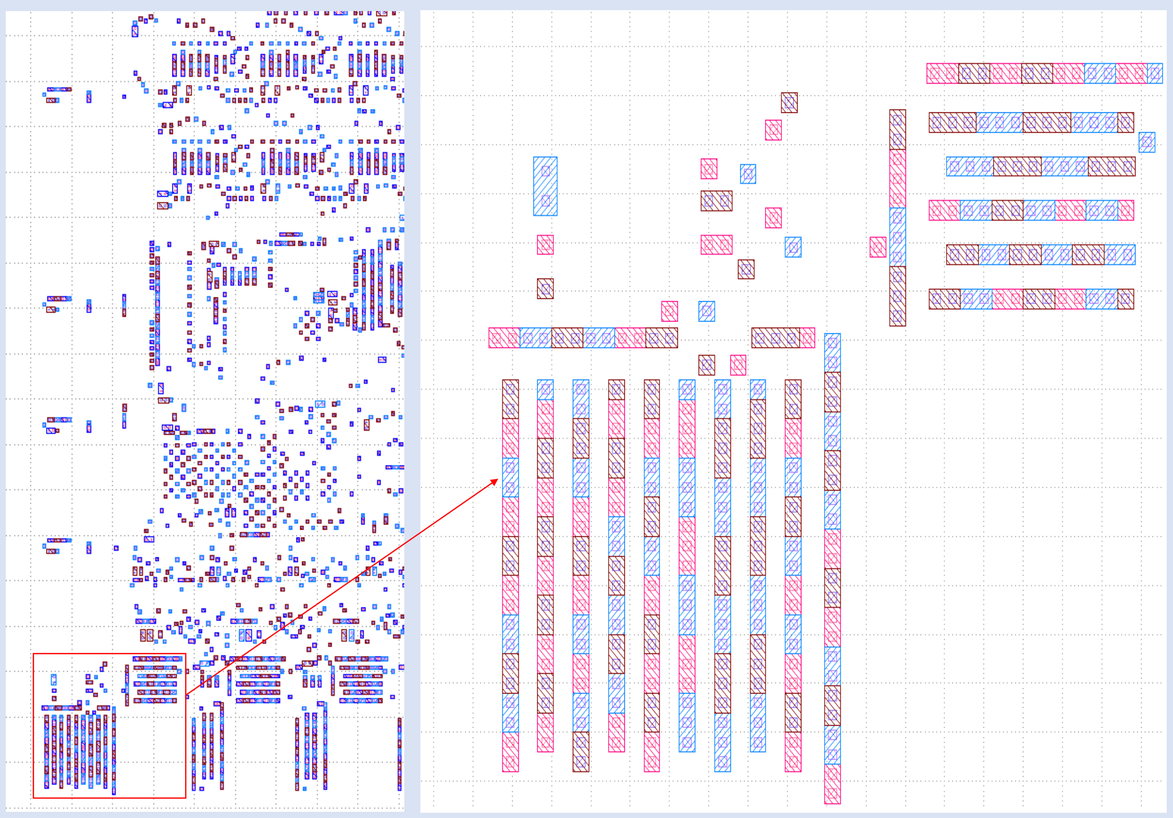


Figure.6. A small part of the grouping and coloring result.

The figure.6 shows the coloring results of some groups in the chip design file office. It can be seen that, by using the proposed method, the original chip vias are divided into several groups. At the same time, each group is evenly split into three layers, while ensuring that the distance between groups meets the technical requirements of DSA.

ACKNOWLEDGMENT

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